REMARKS

Reconsideration of the application as amended herein is respectfully requested. Claims 1 and 9 have been cancelled. Claims 2-8 and 10-17 are pending and remain in this application.

Objections

The Office Action has objected to claims 3, 4, 5, 8, 10, 11, 12 and 13. These claims have been amended to be in a form which Applicant respectfully submits overcomes these objections.

Rejections Under 35 U.S.C. § 112

The Office Action has rejected claims 4-16 under 35 U.S.C. § 112, second paragraph. Applicant has amended these claims (except for claim 9, which has been cancelled), which respectfully submits that the rejections have been overcome.

Rejections Under 35 U.S.C. § 102

The Office Action has rejected claim 2 under 35 U.S.C. § 102(b) as being anticipated by O'Dare et al. or Shen. Applicant respectfully traverses this rejection. Firstly, Applicant notes that O'Dare describes a genetic algorithm for producing test vectors, not for identifying test points. Section 3.1 does describe the use of a heuristic to insert test points that improve random testability. O'Dare discloses that the test points are inserted when the genetic algorithm for determining test vectors stalls and is unable to make progress and that a heuristic is used to determine test point locations. There is nothing in this paper that suggests that a genetic algorithm can be used to determine optimal test point locations.

Likewise, Shen discloses the use of a genetic algorithm for Automatic Test Pattern Generation (ATPG) in sequential circuits. That is, the genetic algorithm disclosed in Shen produces a set of Test Vectors (patterns), made up of stimulus to be applied to a circuit under test and responses to be measured to verify that it has been manufactured correctly. Shen does not recommend or identify changes that should be made to the circuit under test.

In the context of claim 2, neither O'Dare et al. nor Shen disclose that the measure of testability for the IC is determined "*by a combination of fault simulation and fault detection probability*" as required by claim 2. The passage (page 9/2, paragraphs 1-2) in O'Dare cited in the Office Action refers to "*fault simulation*" (lines 3 and 4 of the paragraph 1) and two kinds of "*probabilities*" (the third line from last line of the paragraph 1, and the second line from last line of the paragraph 2). However, the first "*probability*" in O'Dare is the probability "of any chromosome being selected as a parent" and the second "*probability*" in O'Dare is the probability "of any bit being altered". These are not "*fault detection probability*". Finally, the citation from O'Dare does not teach or even suggest that the "measure of testability" for the IC is determined "*by a combination of*" fault simulation and fault detection probability.

The cited section from Shen (section 2.2) talks about three kinds of "*probabilities*". The first "*probability*" in Shen is crossover probability P_c. The second "*probability*" in Shen is bit-crossover probability P_{uc}. The third "*probability*" in Shen is bit mutation probability P_m. None of these are "*fault detection probability*". Moreover, while Shen mentions "*fault simulation*" in section 4, Shen says nothing about determining a measurement of testability for an IC "*by a combination of*" fault simulation and fault detection probability. Based on this, Applicant respectfully submits that claim 2 is in condition for allowance, which is respectfully requested.

The Office Action has rejected claims 3-5 under 35 U.S.C. § 102(b) as being anticipated by Shen. However, claims 3-5 are allowable because they depend from claim 2, which is allowable.

The Office Action has rejected claim 17 under 35 U.S.C. § 102(b) as being anticipated by O'Dare et al. or Shen. As amended, claim 17 makes it clear that the measure of testability for the IC is determined by a *combination of fault simulation and fault detection probability*, which as discussed, is not taught or suggested by either O'Dare or Shen. Thus, Applicant respectfully submits that claim 17 is in condition for allowance.

The Office Action has rejected claims 6-9 and 12-15 under 35 U.S.C. § 102(e) as being anticipated by Harmanani et al. Applicant respectfully traverses this rejection. Applicant first notes that this rejection is improper because Harmanani, which is neither a patent nor a published patent application, cannot be prior art under Section 102(e). Moreover, even if this rejection were proper, independent claim 6 is distinguishable over Harmanani. First, Applicant respectfully submits that Harmanani is directed to a method for generating testable "RTL" designs. See the abstract of Harmanani. RTL, or register transfer language, is a hardware description language used in describing the registers of a digital electronic system, and the way in which data is transferred between them. In contrast, the subject matter of claim 6 is directed to analyzing an integrated circuit design comprised of sequential and combinational logic gates, which is a signficantly lower level of abstraction than present in an RTL design. This helps explain why the method disclosed in Harmanani is distinguishable from the method of claim 6.

For example, contrary to what is stated in the Office Action, Harmanani does not teach anything about determining a "first measure of testability", i.e., step "a". The Office Action points to section 1.2 of Harmanani. Section 1.2, however, does not teach anything about making

such a determination. All section 1.2 teaches is that the method disclosed therein accounts for testability during synthesis, which is not the same as determining a measure of testability. Likewise, Harmanani does not disclose forming sets of test points and determining the size and the number of these first sets, as is required by step "b". The Office Action states that sections 2 and 4.2 of Harmanini provides such a teaching. Applicant respectfully submits that this is incorrect. All section 2 teaches is that portions of the design under test are organized into "test kernals", which Harmanani teaches are the "smallest region that can be tested independently" and that these "test kernals" are "fed directly or indirectly by a psuedorandom pattern generator...." Section 4.2 discusses how a scheduled data flow graph (referred to therein as "DFG") is analyzed to determine "compatibility relations" and that these "compatibility relations" are used to generate an "initial population". However, the claim requires that "a plurality of first sets of test points" be generated. Harmanani does not teach or suggest that test points should be generated such that they are organized into a "plurality" of "sets".

In addition, Harmanani does not disclose evaluating the improvement in the testability (step "c") as part of its process. The Office Action points to section 4.3 as support for this claim element. However, section 4.3 only teaches that the "cost" of datapaths, which has nothing to do with evaluating the improvement in testability. Likewise, Harmanani does not disclose step "h" (which was step "g" prior to amendment) of claim 6, which requires that the first measure of testability be compared to the second measure of testability "to determine whether the selected plurality of first and second pairs of sets converges towards an optimal set to be inserted in the IC as additional test points". The Office Action states that step "g" is disclosed in sections 4.5, 4.6, 5 of Harmanani. Section 4.6 relates to manipulating and merging data, which has nothing to do with comparing different weights of testability. Likewise, section 5 discusses the use of

registers and the cost imposed by such registers. In particular, section 5 teaches that lists of registers are sorted "according to the number of times a register is used in the test mapping" and that the test plan is selected by "choosing the mappings with the highest weight". See page 1077 of Harmanani. The number of registers a test plan might use if unrelated to a measure of testability, which is a measure of the testability improvement that a particular test plan provides. *See Specification*, ¶¶ 20, 23 and 66.

Claims 7-8 and 12-15 are allowable because it depends from claim 6, which is allowable. In addition, Applicant notes that the limitations of claim 7 are not found in Harmanani. The Office Action states that the subject matter required by claim 7 is disclosed in sections 1.2, 2 and 3 of Harmanani. However, the cited sections from Harmanani do not disclose how to determine the size and the number of the sets of test points, let alone the requirements of claim 7. Thus, claim 7 is clearly distinguishable from Harmanani.

The Office Action states that the subject matter required by claim 8 is disclosed in section 4.3 of Harmanani. However, the cited section is entitled "Cost Function and Selection" and relates to the cost imposed by the number and types of components in a data path. Claim 8, however, relates to grouping sets of test points and is not related to determining the cost of a datapath.

Rejections Under 35 U.S.C. § 103

The Office Action has rejected claims 11 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Harmanani. However, claims 11 and 16 are allowable because it depends from claim 6, which is allowable for the reasons discussed above.

Applicant acknowledges that the Office Action has objected to claim 10 as being dependent upon rejected base claim 6. However, because claim 6 is allowable for the reasons discussed above, Applicant respectfully submits that this objection has been overcome and that claim 10 need not be rewritten in order to obtain allowance.

Based on the foregoing, Applicant respectfully submits that this application is in condition for allowance, which is respectfully requested.

Should the Examiner have any questions or comments on the application, the Examiner should feel free to contact the undersigned via telephone.

Respectfully submitted,

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